UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,948,026 B2
DATED : September 20, 2005
INVENTOR(S) : Keays, Brady

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

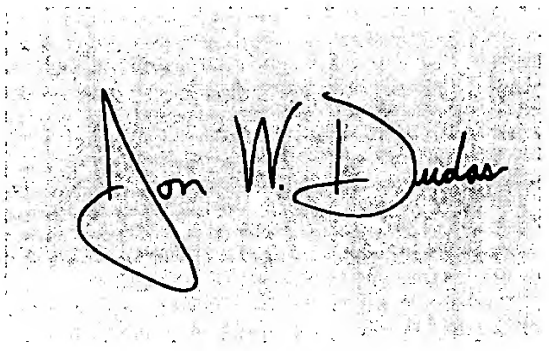
Column 8,
Line 26, "of illustration, only bytes 0, 1, and 2 are shown and the is" should read -- of illustration, only bytes 0, 1, and 2 are shown and the 1's --.

Column 14,
Line 49, "a memory array containing a plurality of floating gale" should read -- a memory array containing a plurality of floating gate --.

Column 16,
Line 46, "gate memory cells arranged in" should read -- gate memory cells arranged in a plurality of erase --.

Signed and Sealed this

Fourteenth Day of March, 2006



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